Silicon Image, Inc

PanelLink™ Technology

Application Note

TFT Data Mapping

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1. INTRODUCTION

This document is a reference in using the PanelLink Transmitter/Receiver chips for TFT applications. Please consult with Silicon Image for the latest information regarding this application.

1.1 One Pixel/Clock Input/Output TFT Mode - VESA® P&D™ and FPDI-2™ Compliant

TFT VGA Output		Input Data Pin			Output Data Pin			TFT Panel Input	
24-bpp	**18-bpp**	**150**	**140**	**100**	**151**	**141**	**101**	**24-bpp**	**18-bpp**
B0		DIE0	D0	D0	QE0	Q0	Q0	B0	
B1		DIE1	D1	D1	QE1	Q1	Q1	B1	
B2	B0	DIE2	D2	D2	QE2	Q2	Q2	B2	B0
B3	B1	DIE3	D3	D3	QE3	Q3	Q3	B3	B1
B4	B2	DIE4	D4	D4	QE4	Q4	Q4	B4	B2
B5	B3	DIE5	D5	D5	QE5	Q5	Q5	B5	B3
B6	B4	DIE6	D6	D6	QE6	Q6	Q6	B6	B4
B7	B5	DIE7	D7	D7	QE7	Q7	Q7	B7	B5
G0		DIE8	D8	D8	QE8	Q8	Q8	G0	
G1		DIE9	D9	D9	QE9	Q9	Q9	G1	
G2	G0	DIE10	D10	D10	QE10	Q10	Q10	G2	G0
G3	G1	DIE11	D11	D11	QE11	Q11	Q11	G3	G1
G4	G2	DIE12	D12	D12	QE12	Q12	Q12	G4	G2
G5	G3	DIE13	D13	D13	QE13	Q13	Q13	G5	G3
G6	G4	DIE14	D14	D14	QE14	Q14	Q14	G6	G4
G7	G5	DIE15	D15	D15	QE15	Q15	Q15	G7	G5
R0		DIE16	D16	D16	QE16	Q16	Q16	R0	
R1		DIE17	D17	D17	QE17	Q17	Q17	R1	
R2	R0	DIE18	D18	D18	QE18	Q18	Q18	R2	R0
R3	R1	DIE19	D19	D19	QE19	Q19	Q19	R3	R1
R4	R2	DIE20	D20	D20	QE20	Q20	Q20	R4	R2
R5	R3	DIE21	D21	D21	QE21	Q21	Q21	R5	R3
R6	R4	DIE22	D22	D22	QE22	Q22	Q22	R6	R4
R7	R5	DIE23	D23	D23	QE23	Q23	Q23	R7	R5
Shift CLK	Shift CLK	IDCK	IDCK	IDCK	ODCK	ODCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Note: For 18-bit mode, the Flat Panel Graphics Controller interfaces to the Transmitter exactly the same as in the 24-bit mode; however, 6 bits per channel (color) are used instead of 8. It is recommended that unused data bits be tied low. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.

Please refer to the Data Sheets for the actual pin numbers for the Input Data Pins of the specific transmitter and Output Data Pins of the specific receiver.

1.2 Two Pixels/Clock Input/Output TFT Mode

TFT VGA Output		Input Data Pins	Output Data Pins	TFT Panel Input	
24-bpp	18-bpp	150	151	24-bpp	18-bpp
B0 - 0		DIE0	QE0	B0 - 0	
B1 - 0		DIE1	QE1	B1 - 0	
B2 - 0	B0 - 0	DIE2	QE2	B2 - 0	B0 - 0
B3 - 0	B1 - 0	DIE3	QE3	B3 - 0	B1 - 0
B4 - 0	B2 - 0	DIE4	QE4	B4 - 0	B2 - 0
B5 - 0	B3 - 0	DIE5	QE5	B5 - 0	B3 - 0
B6 - 0	B4 - 0	DIE6	QE6	B6 - 0	B4 - 0
B7 - 0	B5 - 0	DIE7	QE7	B7 - 0	B5 - 0
G0 - 0		DIE8	QE8	G0 - 0	
G1 - 0		DIE9	QE9	G1 - 0	
G2 - 0	G0 - 0	DIE10	QE10	G2 - 0	G0 - 0
G3 - 0	G1 - 0	DIE11	QE11	G3 - 0	G1 - 0
G4 - 0	G2 - 0	DIE12	QE12	G4 - 0	G2 - 0
G5 - 0	G3 - 0	DIE13	QE13	G5 - 0	G3 - 0
G6 - 0	G4 - 0	DIE14	QE14	G6 - 0	G4 - 0
G7 - 0	G5 - 0	DIE15	QE15	G7 - 0	G5 - 0
R0 - 0		DIE16	QE16	R0 - 0	
R1 - 0		DIE17	QE17	R1 - 0	
R2 - 0	R0 - 0	DIE18	QE18	R2 - 0	R0 - 0
R3 - 0	R1 - 0	DIE19	QE19	R3 - 0	R1 - 0
R4 - 0	R2 - 0	DIE20	QE20	R4 - 0	R2 - 0
R5 - 0	R3 - 0	DIE21	QE21	R5 - 0	R3 - 0
R6 - 0	R4 - 0	DIE22	QE22	R6 - 0	R4 - 0
R7 - 0	R5 - 0	DIE23	QE23	R7 - 0	R5 - 0
B0 - 1		DIO0	QO0	B0 - 1	
B1 - 1		DIO1	QO1	B1 - 1	
B2 - 1	B0 - 1	DIO2	QO2	B2 - 1	B0 - 1
B3 - 1	B1 - 1	DIO3	QO3	B3 - 1	B1 - 1
B4 - 1	B2 - 1	DIO4	QO4	B4 - 1	B2 - 1
B5 - 1	B3 - 1	DIO5	QO5	B5 - 1	B3 - 1
B6 - 1	B4 - 1	DIO6	QO6	B6 - 1	B4 - 1
B7 - 1	B5 - 1	DIO7	QO7	B7 - 1	B5 - 1
G0 - 1		DIO8	QO8	G0 - 1	
G1 - 1		DIO9	QO9	G1 - 1	
G2 - 1	G0 - 1	DIO10	QO10	G2 - 1	G0 - 1
G3 - 1	G1 - 1	DIO11	QO11	G3 - 1	G1 - 1
G4 - 1	G2 - 1	DIO12	QO12	G4 - 1	G2 - 1
G5 - 1	G3 - 1	DIO13	QO13	G5 - 1	G3 - 1
G6 - 1	G4 - 1	DIO14	QO14	G6 - 1	G4 - 1
G7 - 1	G5 - 1	DIO15	QO15	G7 - 1	G5 - 1
R0 - 1		DIO16	QO16	R0 - 1	
R1 - 1		DIO17	QO17	R1 - 1	
R2 - 1	R0 - 1	DIO18	QO18	R2 - 1	R0 - 1
R3 - 1	R1 - 1	DIO19	QO19	R3 - 1	R1 - 1
R4 - 1	R2 - 1	DIO20	QO20	R4 - 1	R2 - 1
R5 - 1	R3 - 1	DIO21	QO21	R5 - 1	R3 - 1
R6 - 1	R4 - 1	DIO22	QO22	R6 - 1	R4 - 1
R7 - 1	R5 - 1	DIO23	QO23	R7 - 1	R5 - 1
Shift CLK	Shift CLK	IDCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

1.3 24-bit One Pixel/Clock Input with 24-bit Two Pixels/Clock Output TFT Mode

TFT VGA Output	Input Data Pins			Output Data Pins	TFT Panel Input
24-bpp	150	140	100	151	24-bpp
B0	DIE0	D0	D0	QE0	B0 - 0
B1	DIE1	D1	D1	QE1	B1 - 0
B2	DIE2	D2	D2	QE2	B2 - 0
B3	DIE3	D3	D3	QE3	B3 - 0
B4	DIE4	D4	D4	QE4	B4 - 0
B5	DIE5	D5	D5	QE5	B5 - 0
B6	DIE6	D6	D6	QE6	B6 - 0
B7	DIE7	D7	D7	QE7	B7 - 0
G0	DIE8	D8	D8	QE8	G0 - 0
G1	DIE9	D9	D9	QE9	G1 - 0
G2	DIE10	D10	D10	QE10	G2 - 0
G3	DIE11	D11	D11	QE11	G3 - 0
G4	DIE12	D12	D12	QE12	G4 - 0
G5	DIE13	D13	D13	QE13	G5 - 0
G6	DIE14	D14	D14	QE14	G6 - 0
G7	DIE15	D15	D15	QE15	G7 - 0
R0	DIE16	D16	D16	QE16	R0 - 0
R1	DIE17	D17	D17	QE17	R1 - 0
R2	DIE18	D18	D18	QE18	R2 - 0
R3	DIE19	D19	D19	QE19	R3 - 0
R4	DIE20	D20	D20	QE20	R4 - 0
R5	DIE21	D21	D21	QE21	R5 - 0
R6	DIE22	D22	D22	QE22	R6 - 0
R7	DIE23	D23	D23	QE23	R7 - 0
				QO0	B0 - 1
				QO1	B1 - 1
				QO2	B2 - 1
				QO3	B3 - 1
				QO4	B4 - 1
				QO5	B5 - 1
				QO6	B6 - 1
				QO7	B7 - 1
				QO8	G0 - 1
				QO9	G1 - 1
				QO10	G2 - 1
				QO11	G3 - 1
				QO12	G4 - 1
				QO13	G5 - 1
				QO14	G6 - 1
				QO15	G7 - 1
				QO16	R0 - 1
				QO17	R1 - 1
				QO18	R2 - 1
				QO19	R3 - 1
				QO20	R4 - 1
				QO21	R5 - 1
				QO22	R6 - 1
				QO23	R7 - 1
Shift CLK	IDCK	IDCK	IDCK	ODCK	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

1.4 18-bit One Pixel/Clock Input with 18-bit Two Pixels/Clock Output TFT Mode

TFT VGA Output	Input Data Pins			Output Data Pins			TFT Panel Input
18-bpp	150	140	100	151	141	101	18-bpp
	DIE0	D0	D0	QE0			
	DIE1	D1	D1	QE1			
B0	DIE2	D2	D2	QE2	Q0	Q0	B0 - 0
B1	DIE3	D3	D3	QE3	Q1	Q1	B1 - 0
B2	DIE4	D4	D4	QE4	Q2	Q2	B2 - 0
B3	DIE5	D5	D5	QE5	Q3	Q3	B3 - 0
B4	DIE6	D6	D6	QE6	Q4	Q4	B4 - 0
B5	DIE7	D7	D7	QE7	Q5	Q5	B5 - 0
	DIE8	D8	D8	QE8			
	DIE9	D9	D9	QE9			
G0	DIE10	D10	D10	QE10	Q6	Q6	G0 - 0
G1	DIE11	D11	D11	QE11	Q7	Q7	G1 - 0
G2	DIE12	D12	D12	QE12	Q8	Q8	G2 - 0
G3	DIE13	D13	D13	QE13	Q9	Q9	G3 - 0
G4	DIE14	D14	D14	QE14	Q10	Q10	G4 - 0
G5	DIE15	D15	D15	QE15	Q11	Q11	G5 - 0
	DIE16	D16	D16	QE16			
	DIE17	D17	D17	QE17			
R0	DIE18	D18	D18	QE18	Q12	Q12	R0 - 0
R1	DIE19	D19	D19	QE19	Q13	Q13	R1 - 0
R2	DIE20	D20	D20	QE20	Q14	Q14	R2 - 0
R3	DIE21	D21	D21	QE21	Q15	Q15	R3 - 0
R4	DIE22	D22	D22	QE22	Q16	Q16	R4 - 0
R5	DIE23	D23	D23	QE23	Q17	Q17	R5 - 0
				QO0			
				QO1			
				QO2	Q18	Q18	B0 - 1
				QO3	Q19	Q19	B1 - 1
				QO4	Q20	Q20	B2 - 1
				QO5	Q21	Q21	B3 - 1
				QO6	Q22	Q22	B4 - 1
				QO7	Q23	Q23	B5 - 1
				QO8			
				QO9			
				QO10	Q24	Q24	G0 - 1
				QO11	Q25	Q25	G1 - 1
				QO12	Q26	Q26	G2 - 1
				QO13	Q27	Q27	G3 - 1
				QO14	Q28	Q28	G4 - 1
				QO15	Q29	Q29	G5 - 1
				QO16			
				QO17			
				QO18	Q30	Q30	R0 - 1
				QO19	Q31	Q31	R1 - 1
				QO20	Q32	Q32	R2 - 1
				QO21	Q33	Q33	R3 - 1
				QO22	Q34	Q34	R4 - 1
				QO23	Q35	Q35	R5 - 1
Shift CLK	IDCK	IDCK	IDCK	ODCK	Shift CLK/2	Shift CLK/2	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE	DE

1.5 Two Pixels/Clock Input with One Pixel/Clock Output TFT Mode

TFT VGA Output		Input Data Pins	Output Data Pins			TFT Panel Input	
24-bpp	18-bpp	150	151	141	101	24-bpp	18-bpp
B0 - 0		DIE0	QE0	Q0	Q0	B0	
B1 - 0		DIE1	QE1	Q1	Q1	B1	
B2 - 0	B0 - 0	DIE2	QE2	Q2	Q2	B2	B0
B3 - 0	B1 - 0	DIE3	QE3	Q3	Q3	B3	B1
B4 - 0	B2 - 0	DIE4	QE4	Q4	Q4	B4	B2
B5 - 0	B3 - 0	DIE5	QE5	Q5	Q5	B5	B3
B6 - 0	B4 - 0	DIE6	QE6	Q6	Q6	B6	B4
B7 - 0	B5 - 0	DIE7	QE7	Q7	Q7	B7	B5
G0 - 0		DIE8	QE8	Q8	Q8	G0	
G1 - 0		DIE9	QE9	Q9	Q9	G1	
G2 - 0	G0 - 0	DIE10	QE10	Q10	Q10	G2	G0
G3 - 0	G1 - 0	DIE11	QE11	Q11	Q11	G3	G1
G4 - 0	G2 - 0	DIE12	QE12	Q12	Q12	G4	G2
G5 - 0	G3 - 0	DIE13	QE13	Q13	Q13	G5	G3
G6 - 0	G4 - 0	DIE14	QE14	Q14	Q14	G6	G4
G7 - 0	G5 - 0	DIE15	QE15	Q15	Q15	G7	G5
R0 - 0		DIE16	QE16	Q16	Q16	R0	
R1 - 0		DIE17	QE17	Q17	Q17	R1	
R2 - 0	R0 - 0	DIE18	QE18	Q18	Q18	R2	R0
R3 - 0	R1 - 0	DIE19	QE19	Q19	Q19	R3	R1
R4 - 0	R2 - 0	DIE20	QE20	Q20	Q20	R4	R2
R5 - 0	R3 - 0	DIE21	QE21	Q21	Q21	R5	R3
R6 - 0	R4 - 0	DIE22	QE22	Q22	Q22	R6	R4
R7 - 0	R5 - 0	DIE23	QE23	Q23	Q23	R7	R5
B0 - 1		DIO0					
B1 - 1		DIO1					
B2 - 1	B0 - 1	DIO2					
B3 - 1	B1 - 1	DIO3					
B4 - 1	B2 - 1	DIO4					
B5 - 1	B3 - 1	DIO5					
B6 - 1	B4 - 1	DIO6					
B7 - 1	B5 - 1	DIO7					
G0 - 1		DIO8					
G1 - 1		DIO9					
G2 - 1	G0 - 1	DIO10					
G3 - 1	G1 - 1	DIO11					
G4 - 1	G2 - 1	DIO12					
G5 - 1	G3 - 1	DIO13					
G6 - 1	G4 - 1	DIO14					
G7 - 1	G5 - 1	DIO15					
R0 - 1		DIO16					
R1 - 1		DIO17					
R2 - 1	R0 - 1	DIO18					
R3 - 1	R1 - 1	DIO19					
R4 - 1	R2 - 1	DIO20					
R5 - 1	R3 - 1	DIO21					
R6 - 1	R4 - 1	DIO22					
R7 - 1	R5 - 1	DIO23					
Shift CLK	Shift CLK	IDCK	ODCK	ODCK	ODCK	Shift CLK*2	Shift CLK*2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE	DE

1.6 Receiver Configuration Settings for 24-/16-bit Color DSTN Applications

Table 1. Output Clock Configuration by Typical Application

DF0	PIX	OCK_INV	PANEL	ODCK (frequency/data latch edge/mode)
0	0	0	TFT/16-bit DSTN	divide by 1 / negative / free running
0	0	1	TFT/16-bit DSTN	divide by 1 / positive / free running
0	1	0	TFT	divide by 2 / negative / free running
0	1	1	TFT	divide by 2 /positive / free running
1	0	0	24-bit DSTN	divide by 1 / negative / blanked low
1	0	1	**NONE**	divide by 1 / negative / blanked high
1	1	0	24-bit DSTN	divide by 2 / negative / blanked low
1	1	1	24-bit DSTN	divide by 4 / negative / blanked low

1.7 Connecting the PanelLink Transmitter/Receiver for 24-/18-bit 1-pixel/clock Input/Output Color TFT Applications

Data to the PanelLink Transmitter is received from the output of the Flat Panel Graphics Controller and should be wired as shown below and in Table 1 above for 24-/18-bit 1-pixel/clock color TFT applications. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.

Graphics Controller		PanelLink						Flat Panel Display	
24-bits	18-bits	SiI150	SiI140	SiI100	SiI101	SiI141	SiI151	18-bits	24-bits
B0		DIE0	D0	D0	QE0	Q0	Q0		B0
B1		DIE1	D1	D1	QE1	Q1	Q1		B1
B2	B0	DIE2	D2	D2	QE2	Q2	Q2	B0	B2
B3	B1	DIE3	D3	D3	QE3	Q3	Q3	B1	B3
B4	B2	DIE4	D4	D4	QE4	Q4	Q4	B2	B4
B5	B3	DIE5	D5	D5	QE5	Q5	Q5	B3	B5
B6	B4	DIE6	D6	D6	QE6	Q6	Q6	B4	B6
B7	B5	DIE7	D7	D7	QE7	Q7	Q7	B5	B7
G0		DIE8	D8	D8	QE8	Q8	Q8		G0
G1		DIE9	D9	D9	QE9	Q9	Q9		G1
G2	G0	DIE10	D10	D10	QE10	Q10	Q10	G0	G2
G3	G1	DIE11	D11	D11	QE11	Q11	Q11	G1	G3
G4	G2	DIE12	D12	D12	QE12	Q12	Q12	G2	G4
G5	G3	DIE13	D13	D13	QE13	Q13	Q13	G3	G5
G6	G4	DIE14	D14	D14	QE14	Q14	Q14	G4	G6
G7	G5	DIE15	D15	D15	QE15	Q15	Q15	G5	G7
R0		DIE16	D16	D16	QE16	Q16	Q16		R0
R1		DIE17	D17	D17	QE17	Q17	Q17		R1
R2	R0	DIE18	D18	D18	QE18	Q18	Q18	R0	R2
R3	R1	DIE19	D19	D19	QE19	Q19	Q19	R1	R3
R4	R2	DIE20	D20	D20	QE20	Q20	Q20	R2	R4
R5	R3	DIE21	D21	D21	QE21	Q21	Q21	R3	R5
R6	R4	DIE22	D22	D22	QE22	Q22	Q22	R4	R6
R7	R5	DIE23	D23	D23	QE23	Q23	Q23	R5	R7
Shift CLK	Shift CLK	IDCK	IDCK	IDCK	VSYNC	VSYNC	VSYNC	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	HSYNC	HSYNC	HSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	DE	DE	DE	HSYNC	HSYNC
DE	DE	DE	DE	DE	ODCK	ODCK	ODCK	DE	DE

Figure 1. 24-/18-bit 1-pixel/clock Color TFT Mode Connection

1.8 Connecting the PanelLink Transmitter/Receiver for 24-/18-bit 2-pixels/clock Input/Output Color TFT Applications

Data to the PanelLink Transmitter is received from the output of the Flat Panel Graphics Controller and should be wired as shown below and in Table 1 above for 24-/18-bit 2-pixel/clock color TFT applications. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.

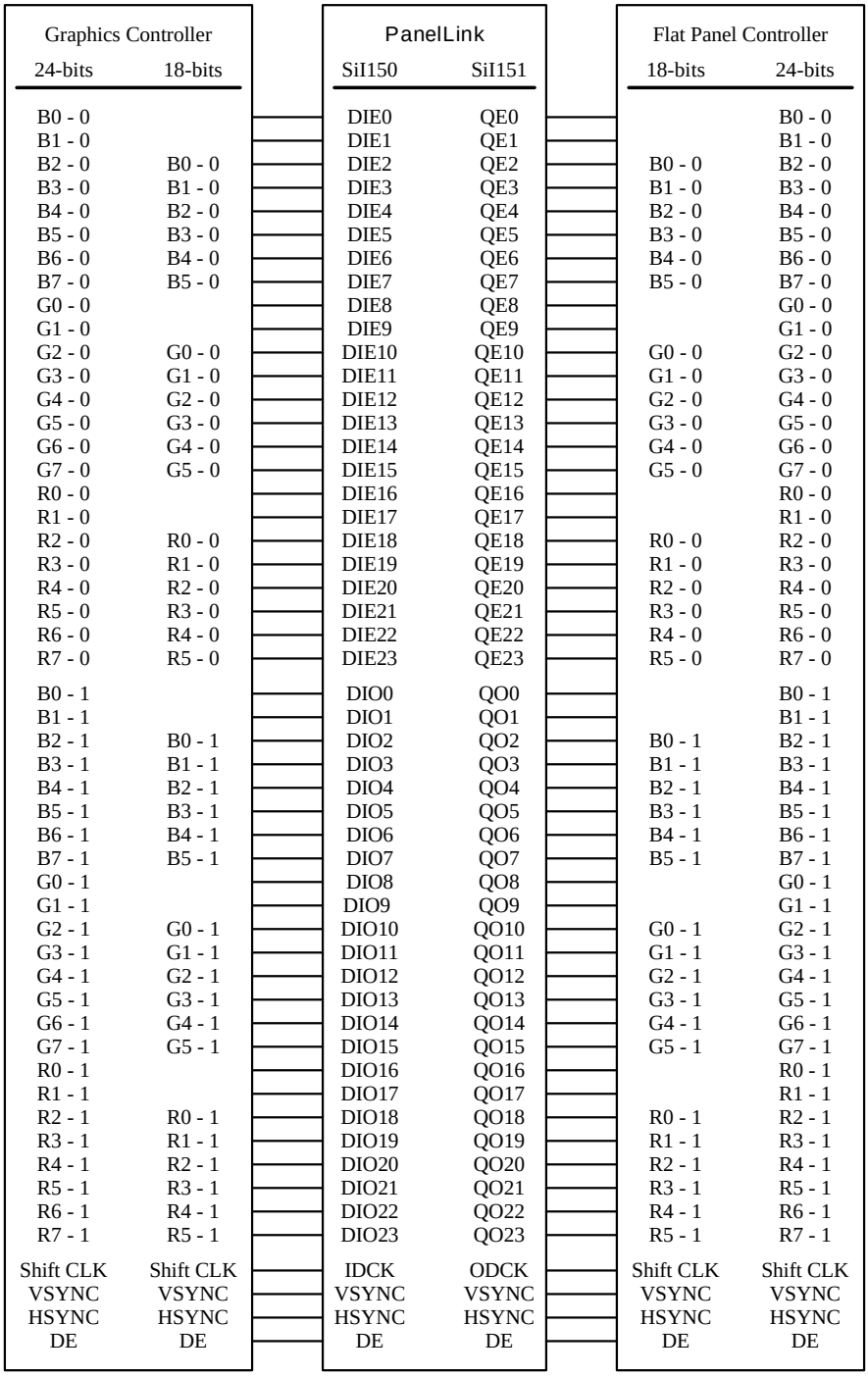
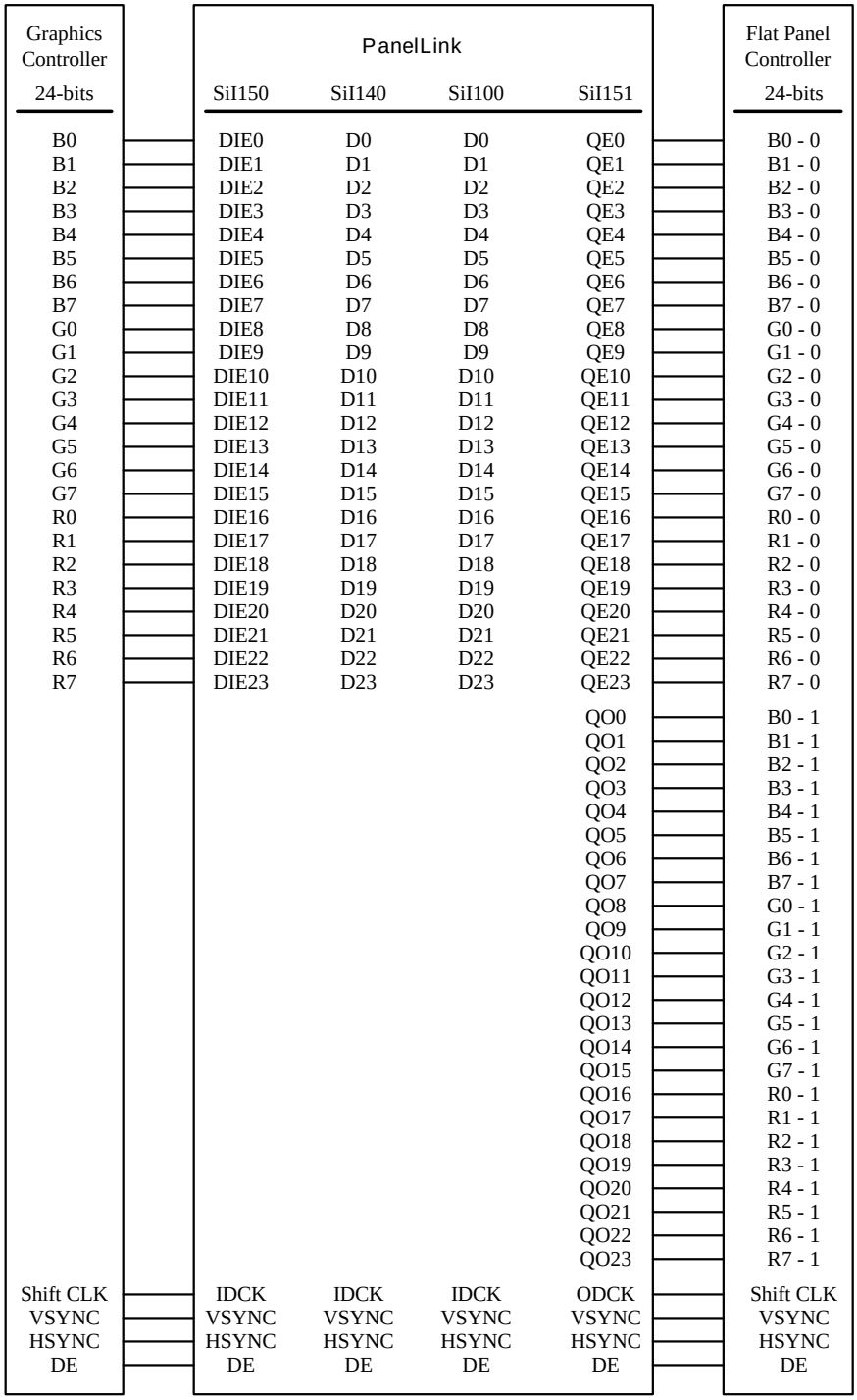


Figure 2. SiI150/SiI151 16-bit DSTN Mode Connection

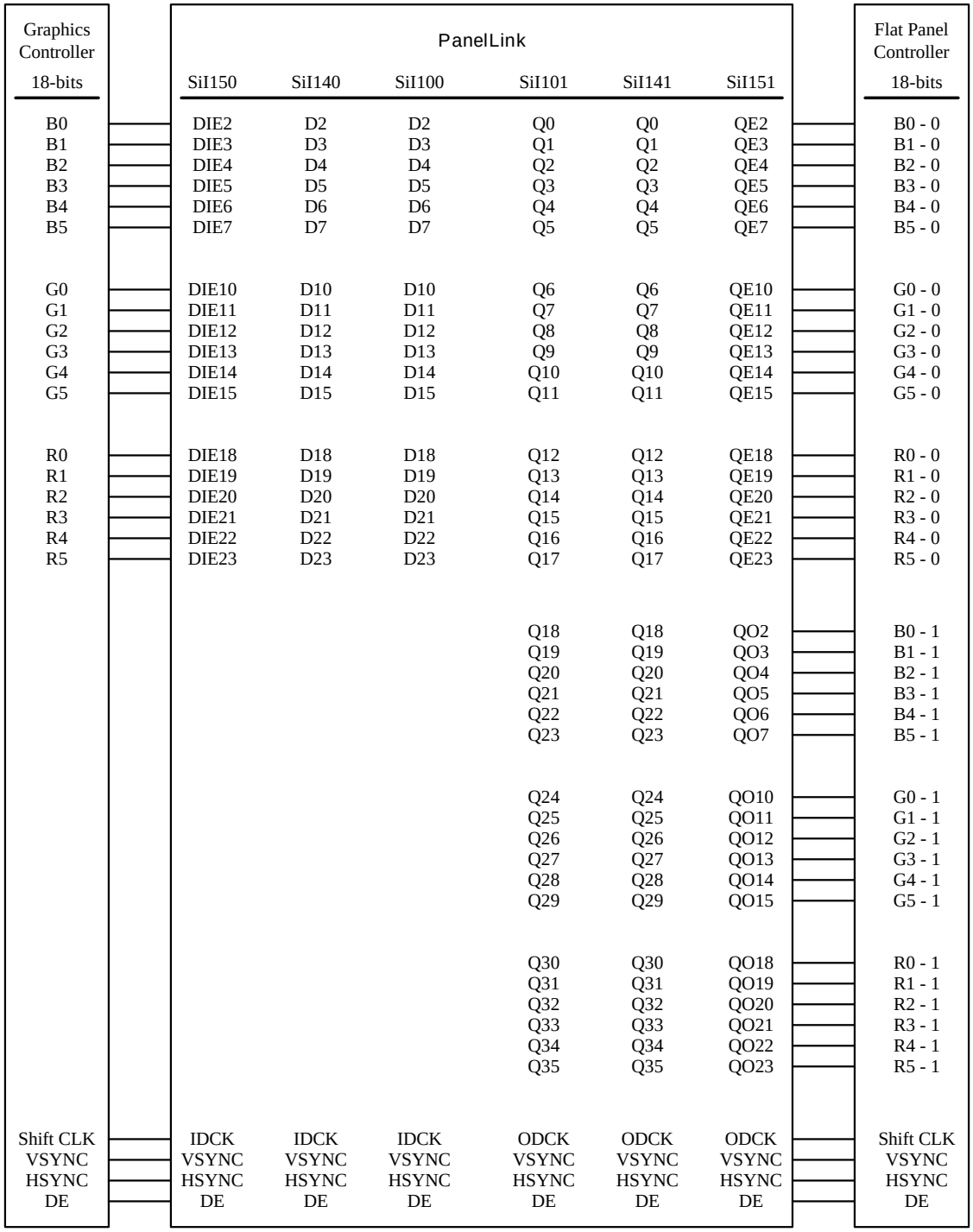
1.9 Connecting the PanelLink Transmitter/Receiver for 24-bit 1-pixel/clock Input to 48-bit 2-pixels/clock Output TFT Applications

Data to the PanelLink Transmitter is received from the output of the Flat Panel Graphics Controller and should be wired as shown below and in Table 1 above for 24-bit 1-pixel/clock input to 48-bit 2-pixels/clock output color TFT applications. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.



1.10 Connecting the PanelLink Transmitter/Receiver for 18-bit 1-pixel/clock Input to 36-bit 2-pixels/clock Output TFT Applications

Data to the PanelLink Transmitter is received from the output of the Flat Panel Graphics Controller and should be wired as shown below and in Table 1 above for 18-bit 1-pixel/clock input to 36-bit 2-pixels/clock output color TFT applications. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.



1.11 Connecting the PanelLink Transmitter/Receiver for 2-pixels/clock Input to 1-pixel/clock Output TFT Applications

Data to the PanelLink Transmitter is received from the output of the Flat Panel Graphics Controller and should be wired as shown below and in Table 1 above for 2-pixels/clock input to 1-pixel/clock ouptut color TFT applications. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.